T1/E1 Loopback Operation for Dallas Semiconductor T1/E1/J1 transceivers

This application note contains an overview of the loopback functions for Dallas Semiconductor T1/E1/J1 transceivers. Loopback modes are useful for diagnostic testing of the device or equipment. In loopback mode, the device loops the signal from one end of the device to the other end of the sending device after it has passed through a network or across a particular link. The signals from both ends can be compared. The discrepancy between the two helps to trace the fault.

Introduction

This application note contains an overview of the loopback functions for Dallas Semiconductor T1/E1/J1 transceivers. T1 and E1 are terms used to refer to the transmission of 1.544 Mbps and 2.048 Mbps over any media.

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Loopback

There are six types of loopback supported by Dallas Semiconductor T1/E1/J1 transceivers.

- 1. Remote Loopback (RLB)
- 2. Local Loopback (LLB)
- 3. Framer Loopback (FLB)
- 4. Diagnostic Loopback (DLB)
- 5. Payload Loopback (PLB)
- 6. Per-Channel Loopback (PCLB)

Remote Loopback (RLB)

This loopback allows the user to test the far end of the equipment link. From the far end equipment, the signal loops through the LIU and the Jitter attenuator.

When the RLB bit of the control register is set to low, then Remote loopback is disabled.

When the RLB bit of the control register is set to high, the Remote loopback is enabled.

In Remote loopback, data input by RTIP and RRING is transmitted back to TTIP and TRING through the jitter attenuator. Data continues to pass through the receive-side framer of the device as it would normally. Data from the transmit-side formatter is ignored.

See Figure 1 for more details.

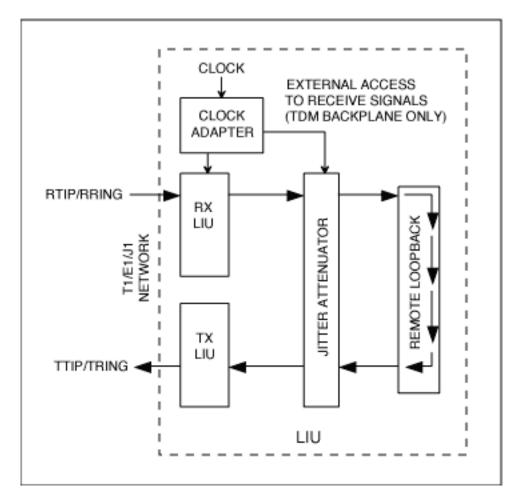


Figure 1. Typical Remote Loopback mode operation

Local Loopback (LLB)

Local loopback allows the user to route data from TSER to RSER and clock from TCLK and RCLK. Local loopback is also called digital loopback, because the device loop backs the data through the digital circuitry of the device.

When the LLB bit of the control register is set to low, then Local loopback is disabled. When the LLB bit of the control register is set to high, then Local loopback is enabled.

In Local loopback, data is transmitted as normal through the transmit side of the transceiver. Data received at RTIP and RRING is replaced with the data being transmitted. Data in Local loopback passes through the jitter attenuator.

Please see Figure 2 for more details.

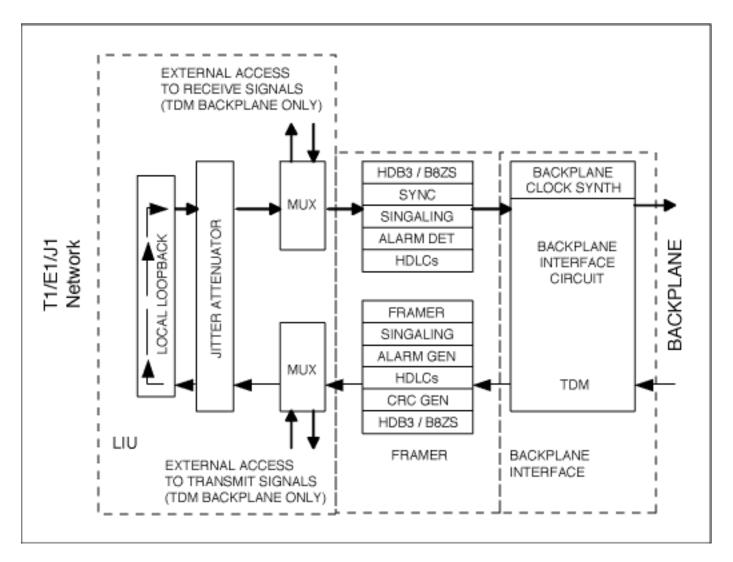


Figure 2: Typical Local Loopback mode operation

Framer Loopback (FLB)

This loopback is useful for testing and debugging applications. In Framer Loopback (FLB), the Dallas Semiconductor devices loop data from the transmit side back plane to the receive side. Data is routed from TSER to RSER and the clock is routed from TCLK to RCLK.

When the FLB bit of the control register is set to low, then Framer loopback is disabled. When the FLB bit of the control register is set to high, then Framer loopback is enabled.

When framer loopback is enabled, the signal from TSER passes through the framer to RSER. This loopback checks the functionality of the framer. In Framer loopback in T1 mode, an unframed all-ones code is transmitted at TPOSO and TNEGO. In E1 mode, Normal data is transmitted at TPOSO and TNEGO.

In Framer loopback mode, all receive-side signals take on timing synchronous with TCLK

instead of RCLKI. When using Framer loopback, RCLK can not be connected to TCLK during this loopback because this causes an inoperative condition.

Please see Figure 3 for more details.

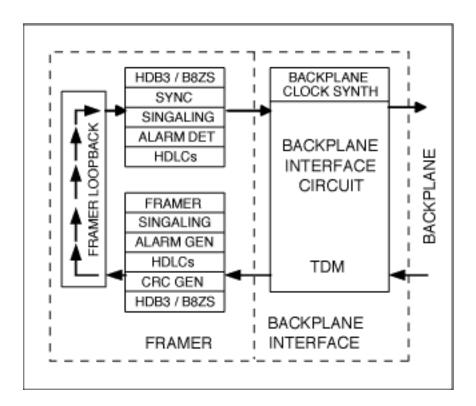


Figure 3: Typical Framer Loopback mode operation

Diagnostic Loopback (DLB)

Diagnostic loopback uses the UTOPIA section of the device only. Diagnostic loopback bypasses the LIU and the framer sections of the device.

Diagnostic loopback enables the transmit data packet to be looped back onto the receive side of the Utopia Bus. This is applicable for Dallas Semiconductor telecom parts like DS2156, DS26101 or DS26102.

In diagnostic loopback, data, clock, and frame-pulse indication generated by the transmit section of the SCT are used instead of the corresponding signals from the physical layer device. Receive physical interface mode should be configured with the same value as transmit physical interface mode. Receive active-edge selection bit should be configured as the opposite edge of that used by the transmit section of the same SCT.

Please see Figure 4 for more details.

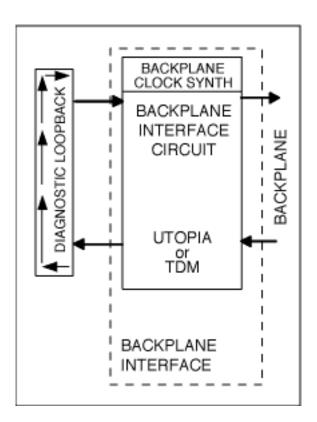


Figure 4: Typical Diagnostic Loopback mode operation

Payload Loopback (PLB)

Payload loopback is useful to verify that the user is receiving a properly formatted data pattern. This loopback re-frames and re-formats the data.

When the PLB bit of the control register is set to low, then Payload loopback is disabled. When the PLB bit of the control register is set to high, then Payload loopback is enabled.

When Payload loopback is enabled, a signal from RTIP/RRING, passes through the LIU and the Framer and loops back to TTIP/TRING. In this loopback mode, the transmitted data is in sync with RCLK instead of TCLK. All the receive side signals continue to operate normally. Data at the TSER, TDATA, and TSIG pin is ignored.

In T1 mode, Payload loopback can be performed both on D4 and ESF framing mode. When the PLB is enabled, the SCT loops the 192 bits of payload data (with BPVs corrected) from the receive side back to the transmit side. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back; they are reinserted by the SCT.

In E1 mode, Payload loopback loops the 248 bits of payload data (with BPVs corrected) from the receive side back to the transmit side. The transmit side modifies the payload as if it was input at TSER. The FAS word; Si, Sa, and E bits; and CRC4 are not looped back; they are reinserted by the SCT.

Please see Figure 5 for more details.

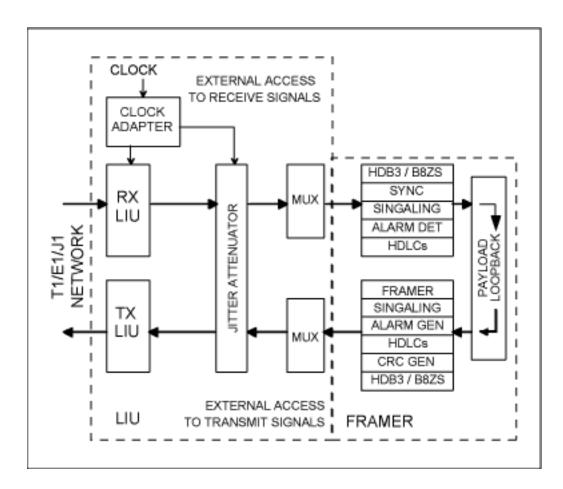


Figure 5: Typical Payload Loopback mode operation

Per-Channel Loopback (PCLB)

Per-Channel loopback is a sub-set of Payload loopback. The data pattern is routed back through the channel that was selected by the user. The per-channel loopback registers (PCLRs) determine which channels (if any) from the backplane should be replaced with the data from the receive side or off of the T1 or E1 line. Per-Channel loopback requires that the transmit clock, receive clocks and frame sync signals to be synchronized. One method to accomplish this is to connect RCLK to TCLK and RSYNC to TSYNC. There are no restrictions on which channels can be looped back or on how many channels can be looped back.

Each of the bit positions in the per-channel loopback registers (PCLR1/PCLR2/PCLR3/PCLR4) represents a DS0 channel in the outgoing frame. When these bits are set to a 1, data from the corresponding receive channel replaces the data on TSER for that channel.

Conclusion

The various loopback modes provided by Dallas Semiconductor transceivers can be very useful in diagnosing data transmission errors on both the line side and the system side of a users application. Decision for implementing loopback should be made based on the customers needs in their application board. For further questions on loopback operation on Dallas Semiconductor parts, please contact the Dallas Semiconductor Telecommunications applications support eam via email telecom.support@dalsemi.com or call 972-371-6555.

More Information

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